AMENDMENTS TO THE CLAIMS

1. (Original) A semiconductor wafer comprising:

a plurality of semiconductor circuits formed on the semiconductor wafer, each semiconductor circuit having a pair of first sides that are parallel to each other, and a pair of second sides that are parallel to each other and perpendicular to the pair of first sides;

a plurality of first saw streets that run parallel to the first sides between a number of the semiconductor circuits;

a plurality of second saw streets that run parallel to the second sides between a number of the semiconductor circuits;

a first metal trace formed between a first saw street and a first semiconductor circuit; and

a second metal trace formed between the first saw street and a second semiconductor circuit, the first saw street lying between the first semiconductor circuit and second semiconductor circuit.

2. (Original) The wafer of claim 1 wherein the first and second metal traces extend across the wafer.

3. (Original) The wafer of claim 1 wherein the first metal trace includes a first section and a second section that lie along side the first saw street, the second section having an extension section that extends away from the second section towards the first saw street.

4. (Original) The wafer of claim 3 wherein the second section has a plurality of extension sections that extend away from the second section towards the first saw street, each extension section having a first leg and a second leg that are

connected together at a first end, and spaced apart and connected to the second section at a second end.

5. (Original) The wafer of claim 4 wherein the extension sections extend varying distances away from the second section towards the first saw street.

6. (Original) The wafer of claim 5 wherein an extension section extends into the first saw street.

7. (Original) The wafer of claim 4 and further comprising:

a reference element formed adjacent to the first and second sections;

a third metal trace that is connected to a first end of the resistive element; and

a fourth metal trace that is connected to a second end of the resistive element.

8. (Original) The wafer of claim 7 wherein the reference element is a resistor.

9. (Original) The wafer of claim 3 and further comprising:

a third metal trace that lies between the first semiconductor circuit and the first saw street; and

an extending section that extends away from the second section towards the first saw street, the extending section contacting the first metal trace and the third metal trace.

10. (Original) The wafer of claim 9 wherein the extending section extends into the first saw street.

11. (Original) The wafer of claim 1 wherein:

the first metal trace runs parallel to the first saw street and then turns and runs parallel to a second saw street; and

the second metal trace runs parallel to the first saw street on an opposite side of the first saw street as the first metal trace, and then turns and runs parallel to the second saw street in an opposite direction as the first metal trace.

12. (Original) The wafer of claim 11 and further comprising:

a third metal trace that runs parallel to the first saw street and then turns and runs parallel to the second saw street on an opposite side of the second saw street as the first metal trace; and

a fourth metal trace that runs parallel to the first saw street and then turns and runs parallel to the second saw street in an opposite direction as the third metal trace on an opposite side of the second saw street as the second metal trace.

13. (Original) The wafer of claim 12 and further comprising:

a fifth metal trace that runs parallel to a third saw street and then turns and runs parallel to a fourth saw street;

a sixth metal trace that runs parallel to the fifth metal trace along an opposite side of the third saw street and then turns and runs parallel to the fourth saw street in an opposite direction as the fifth metal trace, terminating at the first metal trace; and

a seventh metal trace that runs parallel to portions of the fifth and sixth metal traces, terminating at the first metal trace.

14. (Original) The wafer of claim 1 wherein:

the first metal trace is formed around three sides and a portion of a fourth side of the first semiconductor circuit; and

the second metal trace is formed around three sides and a portion of a fourth side of the second semiconductor circuit.

15. (Original) The wafer of claim 14 and further comprising a third metal trace formed around three sides and a portion of a fourth side of a third semiconductor circuit.

16. (Original) The wafer of claim 14 and further comprising a third metal trace formed around both the first semiconductor circuit and a third semiconductor circuit.

17. (Original) The wafer of claim 14 wherein the first and second metal traces are formed in a first level; and further comprising a third metal trace formed around three sides and a portion of a fourth side of the first semiconductor circuit, the third metal trace lying above and being spaced apart from the first metal trace.

18. (Original) A wafer dicing system comprising:

a resistance measuring system that measures the resistances of a plurality of metal traces formed on a wafer; and

a system controller connected to the resistance measuring system that controls the resistance measuring system and processes the resistance values measured by the resistance measuring system.

19. (Original) The wafer dicing system of claim 18 wherein the resistance measuring system includes:

a first multiplexer;

a second multiplexer; and

a resistance detector connected to the first and second multiplexers and the system controller.

20. (Original) The wafer dicing system of claim 19 and further comprising:

a cutting device; and

a cutting controller connected to the cutting device and the system controller.

21. (Original) The wafer dicing system of claim 18 wherein the resistance measuring system includes:

a plurality of resistance detectors; and

a multiplexer connected to the plurality of resistance detectors and the system controller.

22. (Original) The wafer dicing system of claim 21 and further comprising:

a cutting device; and

a cutting controller connected to the cutting device and the system controller.

Claims 23-30 (Cancelled)

31. (Original) The wafer dicing system of claim 18 wherein the system controller outputs a maintenance signal that indicates that maintenance is necessary.

32. (New) A semiconductor wafer comprising:

a plurality of semiconductor circuits formed on the semiconductor wafer, each semiconductor circuit having a pair of first sides that are parallel to each other, and a pair of second sides that are parallel to each other and perpendicular to the pair of first sides;

a plurality of first saw streets that run parallel to the first sides between a number of the semiconductor circuits; and

a plurality of second saw streets that run parallel to the second sides between a number of the semiconductor circuits.

33. (New) The semiconductor wafer of claim 32 and further comprising a first metal trace formed between a first saw street and a first semiconductor circuit.